Application No. 10/721,126

IN THE SPECIFICATION:

After the title, add the following paragraph:

SPECIFIC DATA RELATED TO THE INVENTION

This application is a continuation of U.S. application number 10/026,257 filed December 21, 2001.

Amend as follows:

Page 1, beginning at line 5:

Several different dual damascene processes may be utilized in the fabrication of interconnect structures. One such process is the full via-first ("FVF"), which is illustrated in FIGS. 1 through 4. As shown in FIG. 1, a structure 10 prior to etching may have an interconnect layer 11 in which there is formed a metal interconnect feature ~~18~~ 8. Overlaying layer 11 and feature ~~18~~ 8 is a barrier layer 14. Over barrier layer 14 are two dielectric layers 12 and 13 separated by an intermediate etch stop layer 15. A patterned photoresist ("PR") layer 16 is deposited over top dielectric layer 13.

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The mask films' composition are such that the first mask film has etch properties that are substantially identical to the etch properties of the third mask film while the second mask film has ~~an~~ etch properties that are substantially identical to the etch properties of the fourth mask film. The term "etch properties" as used in this specification are those characteristics of a film or layer composition including the etch rate and etch selectivity for a given etch chemistry and/or etching procedure.

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A sectional view of an interconnect layer of an integrated circuit device or structure 50 is shown in FIG. ~~1~~ 15, and includes a low-k dielectric material including a via dielectric layer 51 and a trench dielectric layer 52 formed over an underlying interconnect layer 53 having a conductive metal 54. Via dielectric, as used in this specification, refers to the portion of a dielectric layer in which a via is formed. A trench dielectric layer refers to a dielectric layer in which a trench is formed. The via dielectric layer 51 is first deposited over a barrier layer 55. The via dielectric layer 51 may comprise any organosilicate or organic low-k dielectric material having a dielectric constant up to about 3.0. Standard dielectric materials and such low-k dielectric materials used are CORAL manufactured by Novellus, BLACK DIAMOND manufactured by Applied Materials, or SILK manufactured by Dow Chemical Company, Inc. An etch stop layer 56 is then deposited over the via dielectric layer 51. A trench dielectric layer 52 is formed over the etch stop layer 56 and comprises the same dielectric material used in the via dielectric layer 51.

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In the present invention, the mask layer 57 has two additional mask films~~,~~ enabling a trench 65 to be first etched in the mask layer 57~~,~~ before the via 63 and the trench 65 are etched through the underlying dielectric material. As shown in FIG.19, The photoresist layer 64 is removed before the features 63 and 65 are etched in the dielectric material. As will be explained in more detail, saving the trench 65 in the mask layer 57 avoids reduction of via size.

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In addition, the etch stop layer in the illustrated embodiment has etch properties similar to the etch property of the second mask film and the fourth mask film 61. Accordingly, the etch stop layer 56 is removed when portions of the fourth mask film 61 and second mask film ~~69~~ 59 are removed as shown in FIG. 23. Alternatively, if the etch stop layer comprises a material having an etch property similar to that of the first mask film and third mask film 60, portions of the mask films 58 and 60 may be removed during the etching procedure for the etch stop layer.

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A trench 75 is then etched through photoresist layer 67 and into the mask layer ~~66~~ 76 through the fourth mask film 73. When the photoresist layer 67 is removed, as shown in FIG. 29, the via 68 and trench 75 are formed in the mask layer ~~66~~ 76. The photoresist material is removed from the via 68, so the misalignment of the trench 75 does not result in the reduction of the size of the via 68.

In the present invention, the trench 75 is patterned in the mask layer ~~66~~, 76 so the photoresist layer can be stripped from the device, before the trench and the via are etched any further. When the photoresist layer 67 is removed the entire width of the via 68 is exposed to the etching procedures, thus the via size cannot be reduced even if the trench has been misaligned.